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POWER-AWARE BUS ENCODING TECHNIQUES FOR I/O AND DATA BUSES: AN EMBEDDED SYSTEM ANALYSIS

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ABSTRACT
Microprocessors with integrated LCD controllers and Flash ROM are used in mobile computer applications. The paper presents a software-only encoding strategy for lowering energy utilisation on the processor-memory bus when showing a picture on the LCD. The idea behind this project is to use the palette as a picture buffer coding table and then redistribute the codes according to the attributes of the images using the LCD controller's translation mechanism. The usefulness of this technique has been empirically demonstrated, with a power decrease of 29% for images with text and 17% for images with graphics. A software-only encoding technique called Compact that minimises CPU transitions is described in the study's second section. The Linux operating system's device driver is modified to carry out Bus-Invert encoding whenever data is read from or written to a Compact Flash file system. Bus transition times can be cut by up to 25% with less software overhead.

Keywords:

INTRODUCTION

Mobile technology has matured into a powerful and culturally significant phenomena. In today's high-tech environment, portable technologies such as PDAs, cell telephones, and GPS voyagers are essential. Energy consumption in microelectronic equipment has become a key concern as processing power grows and product sizes reduce, because high levels of energy usage severely limit item utility.

Semiconductor suppliers provide fully integrated SOC systems for these purposes [1][2][3][4]. On the same semiconductor, these systems combine a RISC microprocessor with several necessary peripheral drivers. By integrating the SOC system with various types of flash memory, I/O modules, power sources, and clock oscillators, a system developer can simply develop a complete mobile system. [5][6]. The use of off-the-shelf standard components decreases overall system costs, shortens the development period, and speeds up product launch. Although these fully

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integrated microcontroller systems are extremely valuable, they limit designers' ability to make aggressive optimizations, such as attempting to decrease system energy usage.

The board also has one or more Static RAM chips, which are utilized as the system memory. The microprocessor was an off item that cannot be altered. Memory modules are also mass-market items with pre-defined interfaces. To hold the displayed visual information, the LCD controller requires a dedicated memory region. The frame reservoir is a storage space that also serves as an interface for application programmers who would like to draw image data on the LCD. The color buffer stores pixel data.

Design Techniques

2.1 Expansion of the Table

If a data result is found in the common value list, the FVE scheme delivers a one-hot code. The height of the common value list, on the other hand, has the following limitation: The number of applications in the common value list for a k-bit broad data lines cannot surpass k. As a result, a value will only be encrypted if it is present in the k-stored elements. A higher likelihood of encoding a data packet value is achieved by storing much more k elements. However, if you try to store more data within the FVE scheme's structure, we'll need extra external command signal. Controllers are particularly expensive to provide since they demand the presence of a free bit on the chip.

2.2 Stored Values' Bit Width.

As previously indicated, we keep the LSB and MSB parts of the data point in separate tables in addition to the complete data value. We changed the bit-width of the inputs from 3 to 28 bits in increments of 1 to discover the best length of the LSB and MSB entries and observed the switching decrease for each case. In Section 6, you'll find the results. Because we use one-hot coding to encode table hits, the amount of packet should be the same as the bit-width of the recorded entries.

2.3 Decorrelator.

Each and every one of the encoding methods developed by researchers employs a decorrelator. The current information value is XORed with the previous information bus number at the encoder's finish. The information bus receives the output of the correlator. The decorrelator XORs the previous and present system bus values at the receiver end to provide the most recent information value.

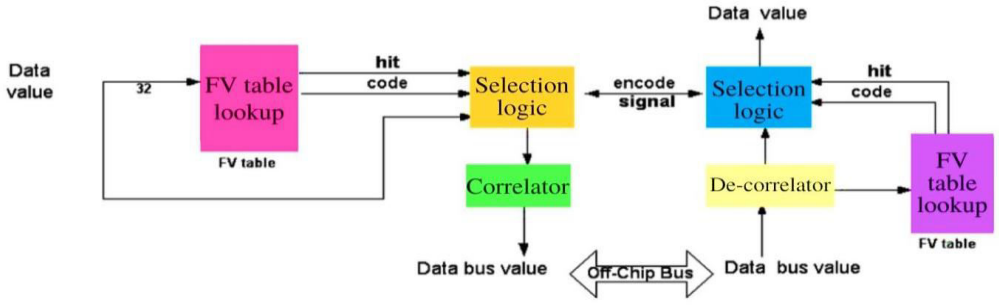

Fig. 1. FV-i encoding technique codec structure.

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2.4.FV-i Encoding

The functioning of an FV-i codec is depicted in Figure 4. By keeping larger tables, the FV-i method overcomes the restrictions of FVE and may thus encode more numeric value. The method mentioned is used by FV-i to maintain larger tables. When I equals 0, the FV-i scheme transforms into the FVE scheme.

2.5.FV-i-MSB-j Encoding

This method allows us to encode the whole piece of data as well as its MSB portion using an FV repository and an MSB table. All of the details are in the FV table.

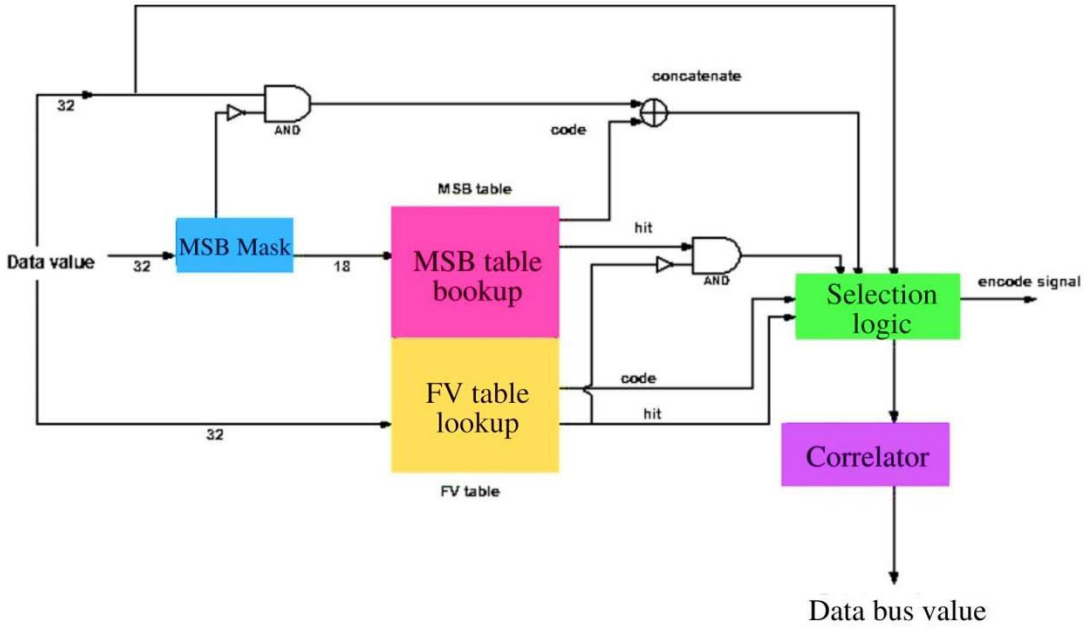

Fig. 2. Structure of the FV-i MSB-j encoder.

Here, r is a value that the designer decides on and is limited by the rule that r k, where k appears to be the length of the data-bus. Three separate metrics are used to assess this scheme's effectiveness. The appropriate tables are increased using the variables I and j.

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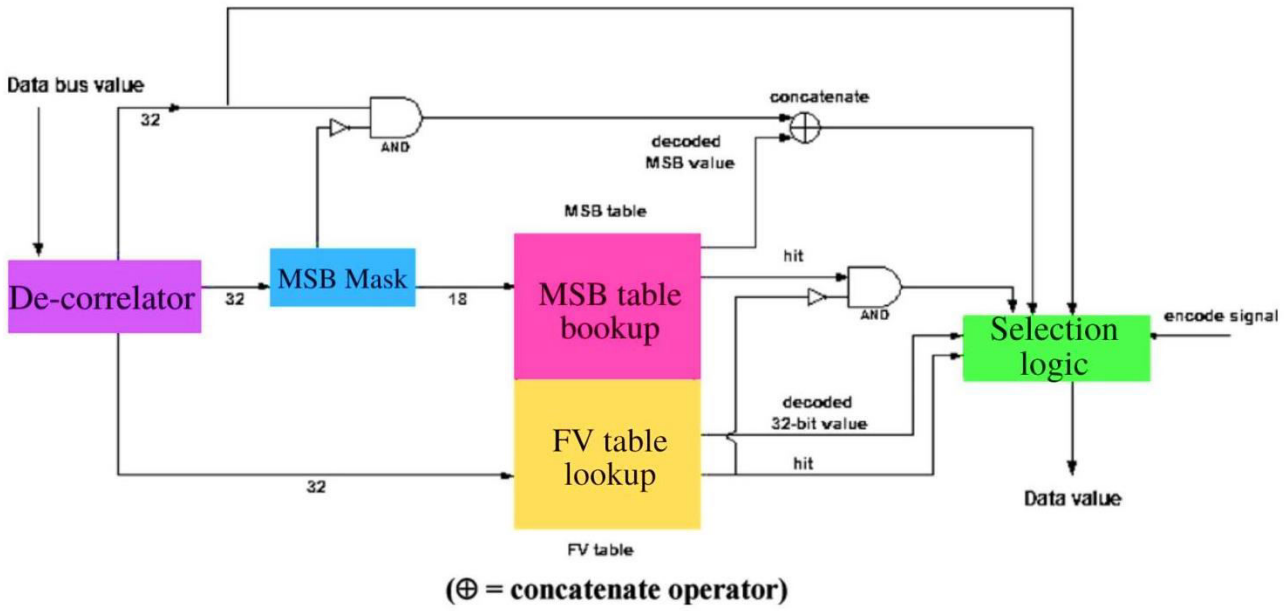

Fig. 3. FV-i-MSB-j decoder.

EXPERIMENTAL SETUP

For our studies, we updated the sim-outorder simulation from the SimpleScalar toolset . We altered the amount of bits collected in MSB/LSB based methods from 3 to 28 values in steps of 1. Finally, we determined the amount of bits to be captured for each strategy calculated on the basis drop in power switches for various benchmarks. We employed a variety of tests that are typical of both micro and desktop applications to assess the efficacy of our encoding strategies.

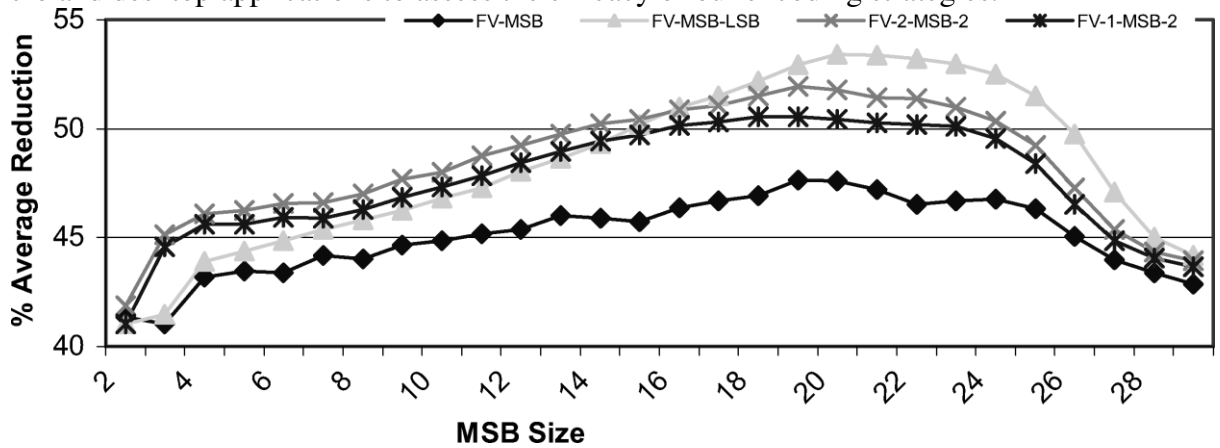

Fig. 4. Switching activity is reduced on average for different MSB lengths.

SPECINT apps are typically run on desktop-style platforms with many cache memory levels. As a result, when running SPECINT apps, we chose a second-level cache. To closely mimic widely deployed modules, we chose design without L2 cache when executing embedded software applications. When running SPECINT programmes with the ref dataset, we used a 64KB L2 cache. The command and information caches' block sizes were set to 32 bytes.

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4.1.. ENERGY

4.1.1. Model for Bus Power

For each bus route in this formula, Cmetal represents the impedance of the metal connector. Based on the information given, a value of 20 pF is predicted. Cbus provides the effective inductive load that must be supplied during a bridge transaction.

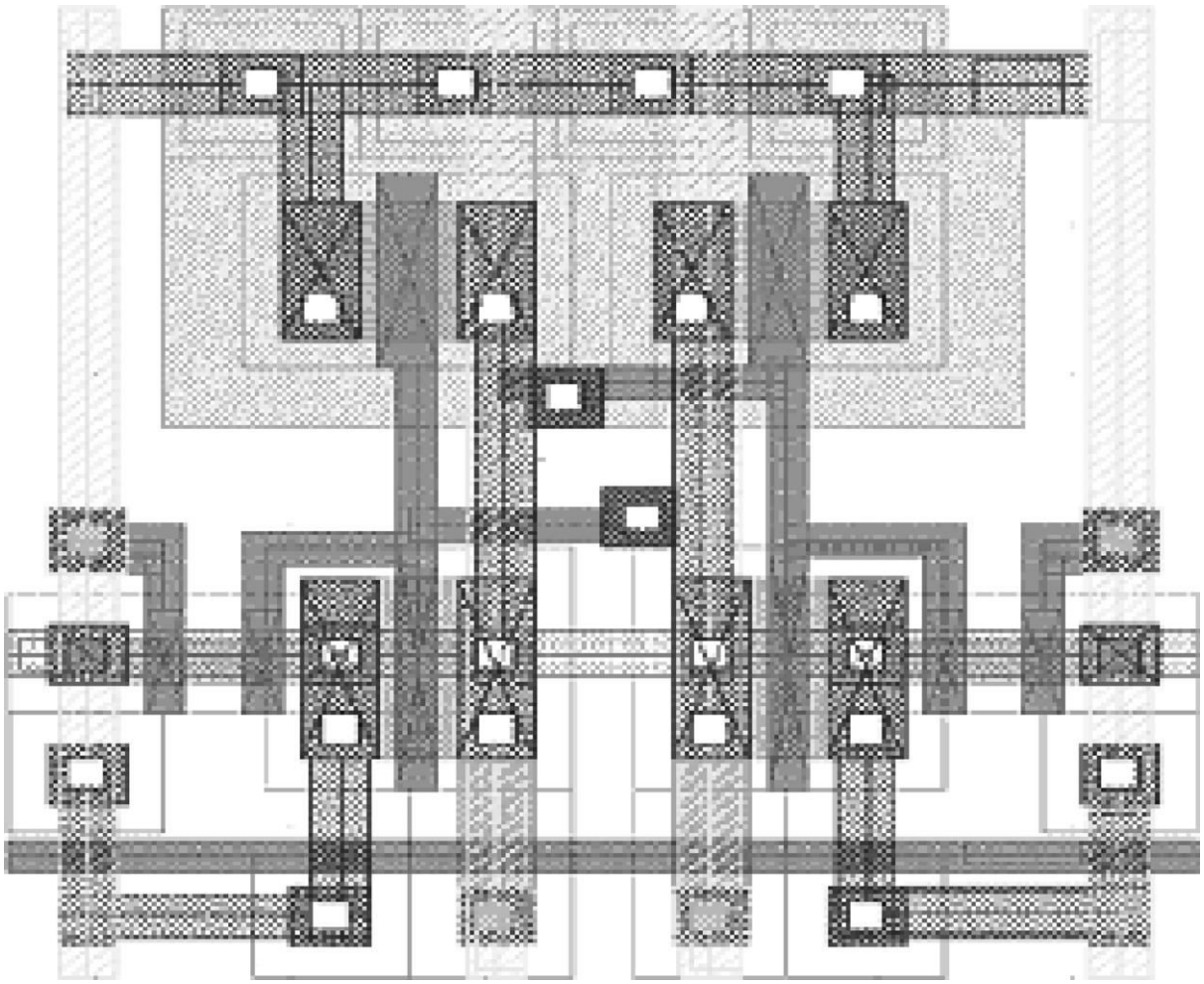

Fig. 5. CAM cell.

4.2 Coder's Energy

We go over each of the codec elements in greater outlined in the subsequent paragraphs. Tables, ecorrelator, decision logic, and system logs are the four primary components of our codec design.

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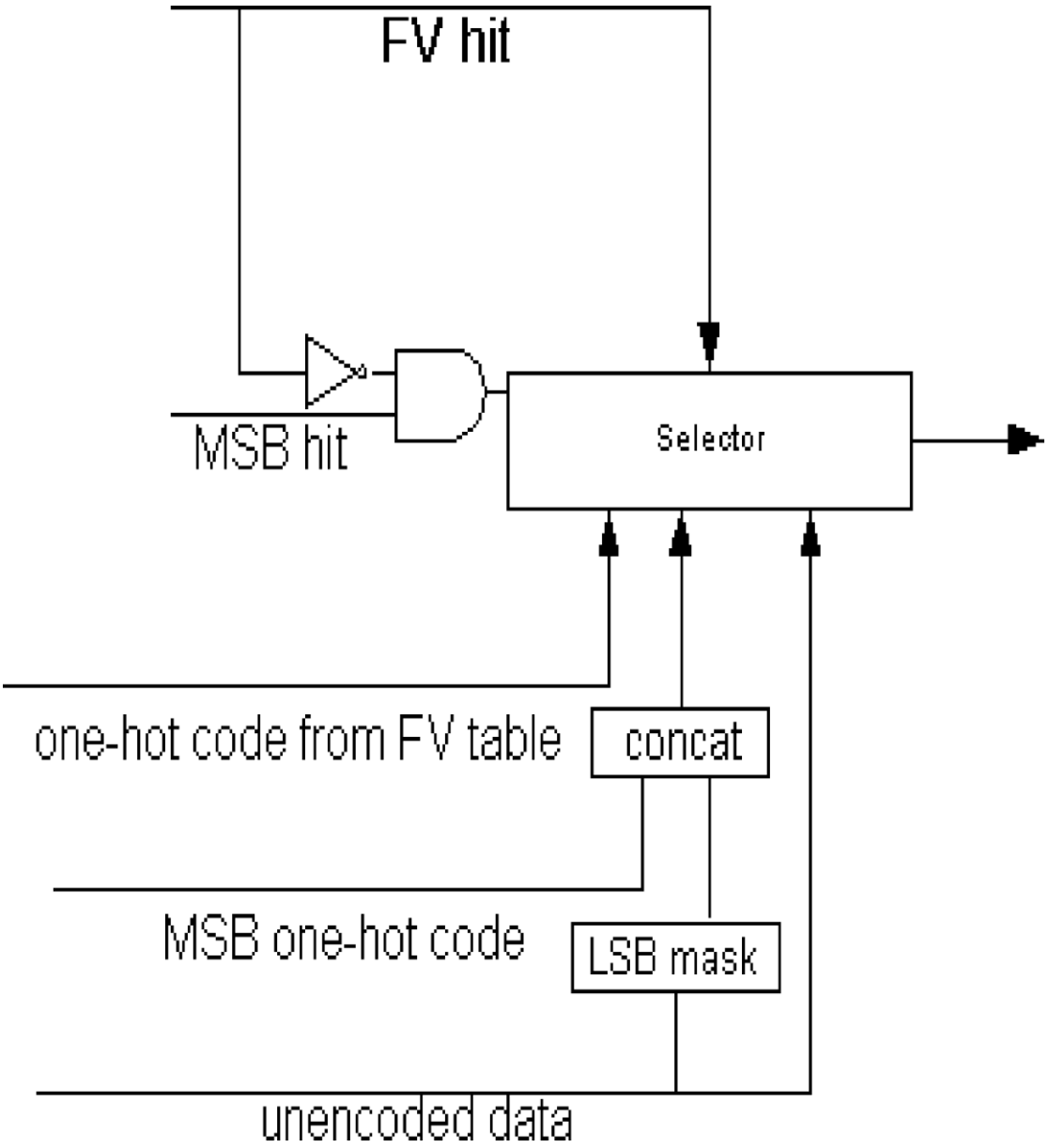

Fig. 6. The power consumption in the logic circuits (LSB mask and MSB hit signal) plus the energy consumed by the selector (18 0.095pJ + 1.33pJ = 3.04pJ) make up the selection logic for FV-i-MSB–j.

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FV hit	MSB hit	Selector's output
1	X	One-hot code
0	1	MSB-code + lower portion
0	0	Unencoded data

Fig. 7. FV-i -MSB-j selection logic input and output values.

Table I. Codec components use a lot of energy.

Component	Selection logic	XOR gates	Timestamps	32-bit, 32 - entry table
Energy	3.04pJ	0.095pJ Transition pair	0.07pJ	13.6p
Delay	0.2 ns	0.1 ns	0.5 ns	0.2 ns

Conclusions

To lower the energy usage of the memory and I/O bus, two technologies were tested on an embedded platform with an LCD and Flash ROM. The shared memory was coded using the palette, which is the LCD controller's interpretation technique. The suggested solution re-encoded the palettes and updated the pixel buffer entries based on their picture correlation. The issue was framed as a state allocation problem, and an effective heuristic approach built on SA was offered to solve it. The efficiency of this strategy was demonstrated by experimental data showing a 29 percent loss in power for text images and a 17 percentage loss for graphics-mode images.

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