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Analysis of True Single Phase Clocked Flip-Flop at 180 nm Technology

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ABSTRACT

One of the most common as well as an important building block in any digital circuits are the Flip flops. Design is affected by factors such as power, performance, and area. For a systematic design these three must be optimized. When designing within time constraints, throughput and power optimization are the main priorities. Power, Performance and area parameters can be optimized using a plenty of techniques. This study discusses every flip flop design already in use before analysing a 15-transistor, high-speed, low-power flip flop using 180nm technology. To minimize floating internal nodes and reduce dynamic consumption of power, the TSPC FF uses static CMOS and complementary pass transistor circuitry. Flip Flop is implemented using the Cadence Virtuoso tool. Flip Flop's clock frequency is 500MHz, and the supply voltage VDD is 1V. The 180nm technology was utilized in the implementation.

Keywords: Flip Flops, true single phase clocked flip flop, setup time, hold time, power dissipation.

INTRODUCTION

Flipflops are fundamental elements of memory (data storage). These are used for storing 1 bit, either 0 or 1. It has two stable states, hence it is also known as bistable multivibrator. Flip Flop has two outputs which are always compliment to each other. Flip Flop can be used as frequency divider. A binary state can be maintained indefinitely in a flip flop till power is switched off. The states of Flip Flop are switched with the help of an input signal. The variations among different types of flip-flops are in: the number of inputs possessed by the Flip Flop and the way in which the binary state is affected by the inputs to determine type of the Flip Flop [1-2].

SR FF

For the construction of a Flip Flop two NAND gates or two NOR gates can be used. These are shown in the logic diagrams given below. Output of one gate is cross coupled to the input of other for creating a feedback path. Thus, the circuits are categorized as asynchronous sequential circuits. Every Flip-Flop comprises of two inputs, set and reset and consist of two outputs, Q and Q'. Other more complicated types of circuit can be built from these basic flip flop.

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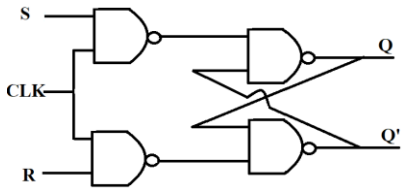

Fig. 1. SR FF using NAND gate
Characteristic equation of SR FF is:
QN+1 = S + R' QN

JK FF

One of the most utilised Flip Flops in digital circuits is the JK Flip Flop. When coming to SR Flip Flop, it has two drawbacks: a. The condition having both inputs zero is avoided. b. The incorrect latching action takes place, when enable is 1 and the Set, Reset input changes their state. Thus JK FF is used to overcome these drawbacks in SR FF.

The J K Flip Flop has the advantage of being a universal Flip Flop. Unlike J K Flip Flop, the initials 'S' and 'R' in SR Flip Flop stand for Set and Reset. The Flip Flop design is distinguished from other forms of flip flops by the use of separate letters J and K.

The way of working of both JK and SR Flip Flop is almost same. The only difference between the two is in JK flip flop, there are no invalid states even when both the inputs are taken as 1 while in SR Flip Flop when both the inputs are taken as 1 the output will be invalid state. A problem that arises in JK Flip Flop is the Race Around Condition i.e., for both inputs taken as 1 along with a high clk for a longer period, the output will toggle if the clk is high. This condition leads to an unstable or uncertain output [2].

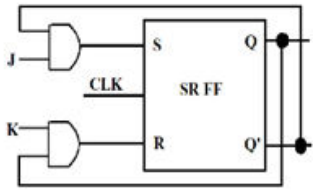

Fig. 2. JK FF from SR FF
Characteristic equation of JK FF: QN+1 = J QN'+ K' QN

D FF

The D flip-flop can hold data into its internal storage and it is also known as gated D-latch. The D Flip Flop is designed by adding an inverter between the 'S' i.e. set and 'R' i.e. the reset input of SR flip flop. As a result, S and R can never both be identical to one simultaneously. The D Flip Flop is also called as a Data Latch or just a D Flip Flop. A delay line, zero-order hold, or memory cell can all be used to describe the D flip-flop.

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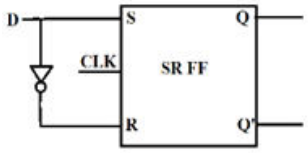

Fig. 3. D FF from SR FF
Characteristic equation of D FF: QN+1 = D

T FF

A JK flip flop can be used to create a T flip flop by connecting both inputs together; this transforms the JK flip flop into input pin T. As a result, T flip flops are referred to as single input JK flip flops. The T Flip Flop generates an output frequency that is half that of the input frequency. Thus it acts as a frequency divider circuit. For example, the output frequency will be 4 MHz if the input is 8 MHz. The major application of T Flip Flop is that it is used as counter and in control circuit [2-3].

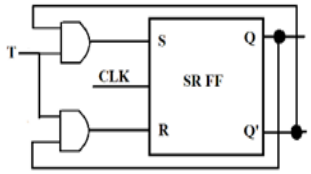

Fig. 4. SR FF from T FF
Characteristic equation of T FF: QN+1 = T QN

Existing Flip Flop design :

- TGFF (Transmission Gate FF)
- SRFF (Set Reset FF)
- ACFF(Adaptive Coupling FF)
- TCFF (Topologically Compressed FF)
- SAFF (Sense-Amplifier-based FF)
- LRFF (Logic Reduction FF)
- TSPC FF (True Single Phase Clocked FF)

Many Flip Flop designs have been constructed in the past, however contemporary designs focus on switching from ultra-high-speed toggling to ultra-low-power operations. The current focus is on lowering power usage as well as switching power. First, a detailed examination of existing FF concepts is offered.

Existing Flip Flop designs:

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- TSPC FF (True Single Phase Clocked FF)

TG FF

Advantages:

i) The most often used Flip Flop is one that is based on a transmission gate (TGFF).

Disadvantages:

i) As data switching activity increases, the slave latch's data contention problem worsens, diminishing the benefits of power savings.

ii) Because the master latch's level restoring circuit pair takes longer to set up, the setup time is longer.

iii) When specific input and internal node combinations occur, a power leaking problem arises.

iv) The requirement for complementary signals places an excessive amount of work on the clock signal.

v) Dynamic power dissipation is substantial even when data switching activity is modest.

vi) The clock drives 12 transistors in a TG flip flop, which results in a large capacitive load. Due to the significant capacitive loading effect, even with a modest switching factor, the dynamic power consumption is substantial.

vii) Since TGFF uses two clock phases as two clock phases require additional circuitry, and an adequate clock distribution method is also required to reduce clock latency and skew problems. Additional circuitry is needed to produce two clock phases, and the clock distribution method is also required and must be efficient to minimise clock jitter and skew problems.

True Single Phase Clocking FF solutions have been developed to overcome the restrictions of employing two phases of the clock. Both the master and slave of a TSPC Flip Flop employ a single-phase clock [4-5].

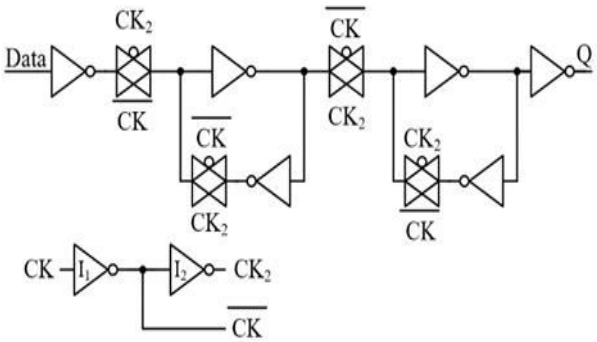

Fig. 5: TG FF Schematic FPGA.

SR FF

Advantages:

i) To facilitate single clock phase operations, this latch is used instead of a TG-based latch.

ii)Lowers the circuit complexity of TG based Flip flop

iii)Alleviates clock signal loading problem present in TG Flip Flop.

Disadvantages:

i) Even when the input remains static, dynamic power consumption is substantial.

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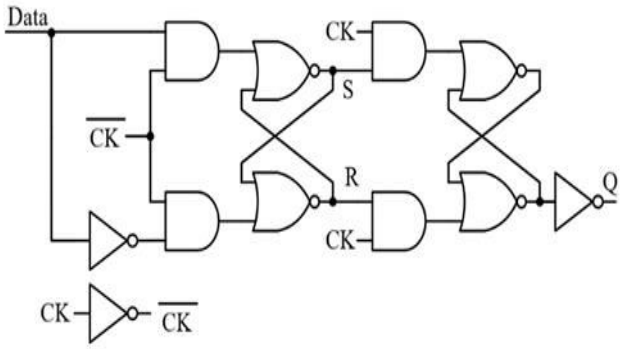

Fig. 6: SR FF Schematic

AC FF

Advantages:

i) It employs a simpler PMOS latch design, resulting in a significant increase in power efficiency.
ii)Because of PMOS latch design even the loading on the clock network is lighter[4].

Disadvantage:

i) The power delay performance of pulse generation circuits is poor because they are subject to process fluctuations.

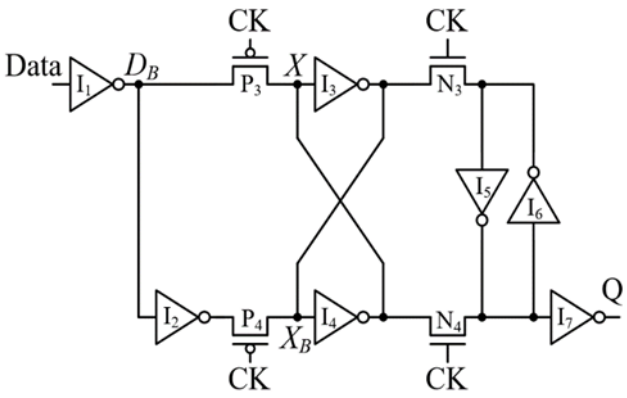

Fig. 7: AC FF Schematic[4]

TC FF

Advantages

i) It only has one phased clock.
ii) The total number of transistors has also been reduced to 21.
iii)Significant improvement in power consumption and area reduction.
iv) The leakage power is reduced when floating nodes are not present.

Disadvantages

i) The TCFF design's timing performance suffers as a result of the reduction in power consumption.
ii) There are just two PMOS transistors that are directly connected to VDD due to a weak pull-up network, which increases setup time. Although increase in the size of PMOS transistors helps to

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solve this problem, it has a negative impact on power consumption.

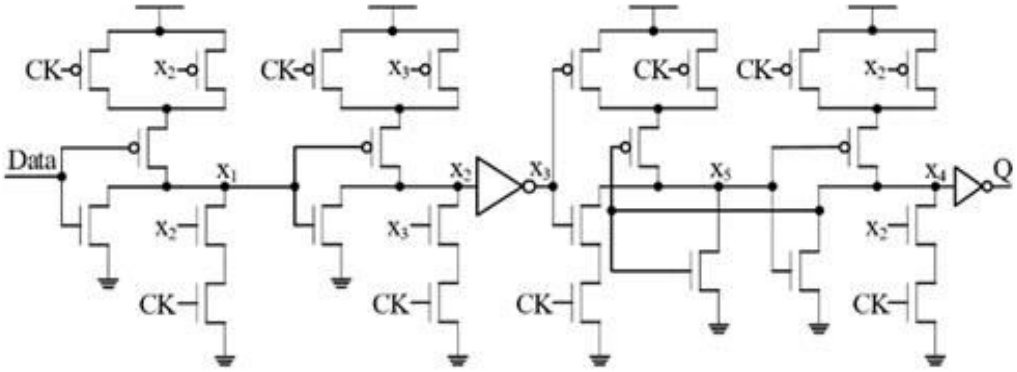

Fig. 8: TC FF Schematic [2]

LR FF

Advantages

i)Use of single phased clock signal.

ii) The required number of transistors for FF design has been decreased to 19, which leads in reduction of power consumption and size.

iii) There is a reduction in setup time.

iv) There is a reduction in leakage power because there are no floating nodes in the architecture [5].

Disadvantages

i) In a pipelining structure, a maximum propagation delay is established for a combinational block due to the lower hold time.

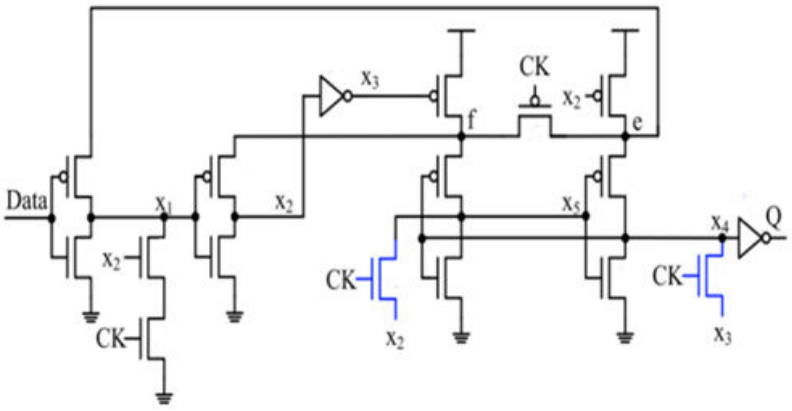

Fig. 9: LR FF Schematic [3]

TSPC FF

Advantages

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i) It gets rid of the LRFF's discharge routes and improves the dynamic power consumption metric.
ii) Analyzed and compared to different designs, average power consumption, delay and power delay product showed that it is superior.
iii) The setup and hold times are also the best when compared to other designs.
When compared to other designs, the TSPC Flip Flop performs better in every metric.

LITERATURE BACKGROUND

The TSPC Flip Flop Design Using Circuit Simplification Method on LR Flip flop is discussed below:

Designing TSPC FF from LR FF

LRFF MOS circuit schematic with 19-transistors is depicted in Fig 9. The schematic of the MOS circuit of a 17-transistors TSPC Flip Flop is shown in Figure 10. The solid and dotted views illustrate the OFF and ON states of each transistor during the data latching operation, respectively in Fig 10, which represents the OFF and ON states during the data latching process of each transistor. Path A passes through an N6 transistor when data is set high. Path B through the series-connected N8 and N7 transistors is used when nodes x2 and CK are both high, with node x2 being high if data is high. When channel BA is open and both CK and data are high, node x1 discharges to zero. As a result, the probability of node x1 discharging through path B is half that of channel A when the clock signal's duty cycle is 50% and the data is significant. The clock signal also drives transistor N8 in path B, which compensates for capacitive loading, resulting in the power consumption even when way B isn't draining the node x1, i.e., when node x2 is low. As a result, by deleting path B from an LR Flip Flop's master stage, the propagation delay, power consumption, as well as the area occupied by the Flip Flop, can be reduced without jeopardising the Flip Flop's performance and Flip Flop's functioning. Almost all performance characteristics have increased when compared to LRFF, including clock- to-Q propagation delay (C- Q), data-to- Q propagation delay (D-Q), power delay products PDPC-Q, setup time, average power dissipation, , and PDPC-Q [2-6].

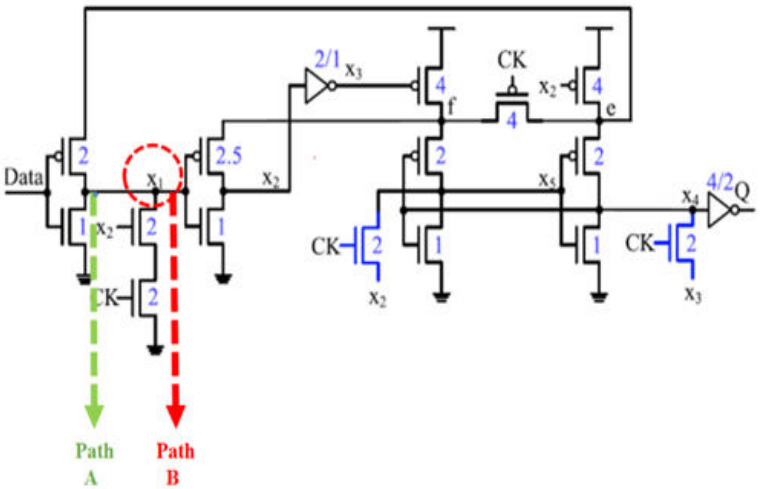

Fig. 10: Discharge Path for node x1 in LR FF

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Working of TSPC Flip Flop

Mechanism of the data latching in the 15-transistor TSPC FF is depicted after eliminating route B and I2 inverter. When the data signal is 0, the data latching procedure is shown in Figures 11.a and 11.b. The Figures 11.c and 11.d show the data latching technique when the data signal is low. The master latch is enabled and during a transparent state when the CK signal is low, as shown in Fig.11. a. Nodes x2 is set to low and node x3 is set to high, respectively. The slave latch has no effect on the output and is in an inactive and hold condition. The non-signal inputs x2 and x3 are provided to P2 and P4 transistors, respectively, and their role is to govern the v2 and v1 pseudo VDD nodes. Nodes v1 and v2 are connected by Pb, a clock-controlled transistor, so that both can achieve VDD. When CK levels are high, the master latch is inactive and held, while the slave latch is active and transparent, as shown in Fig 11.b. In nodes x3 and x2, through Pass transistors N1 and N4, the outputs of the master latch are passed to the slave latch. Nodes x3 and x2 must maintain their values for the slave latch's output state to change for a minimum period of time known as hold time. Node v2 does not achieve VDD since Pb is turned off, so any data changes have no effect on x3 and x2. As a result, the master latch is unresponsive to data changes. Node x2 remains low even though data becomes high by discharging through transistors N3 and N4. x3 Node is kept high by charging the transistors P1, P2 and N1. As a result, no internal floating nodes exist. Data high latching works in a similar way, as seen in figs. 11.c and 11.d[7-8].

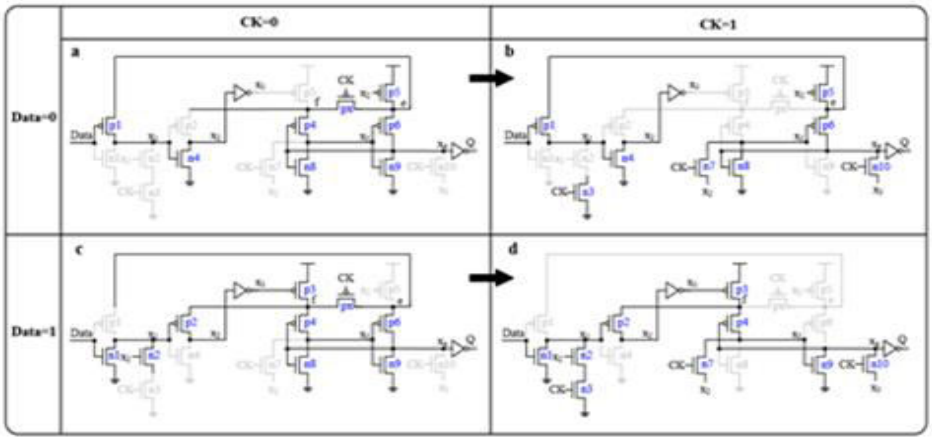

Fig. 11: Data Latching Process in LR FF[3]

TSPC PERFORMANCE EVALUATION

The TSPC FF was simulated in Cadence Virtuoso software using 180 nm technology. Its schematic was made and then AC, DC and transient analysis was done. The functionality was verified using transient analysis and then delay was calculated. Hold time and setup time was also calculated using Cadence. Total power was also computed.

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All the simulations are shown in the figure below.

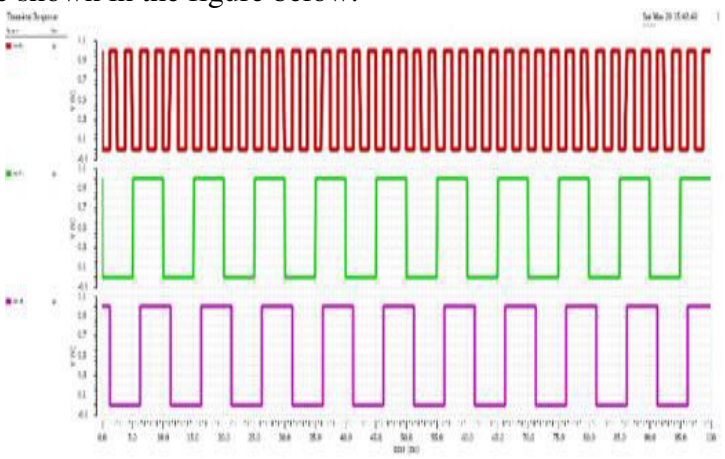

Fig. 12 : Transient Analysis of TSPC FF

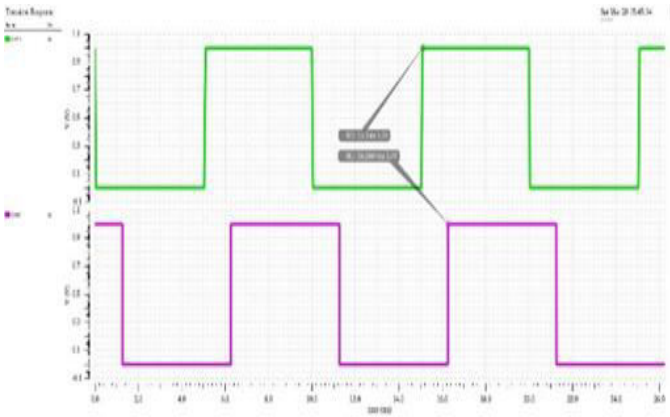

Fig. 13: Delay Calculation

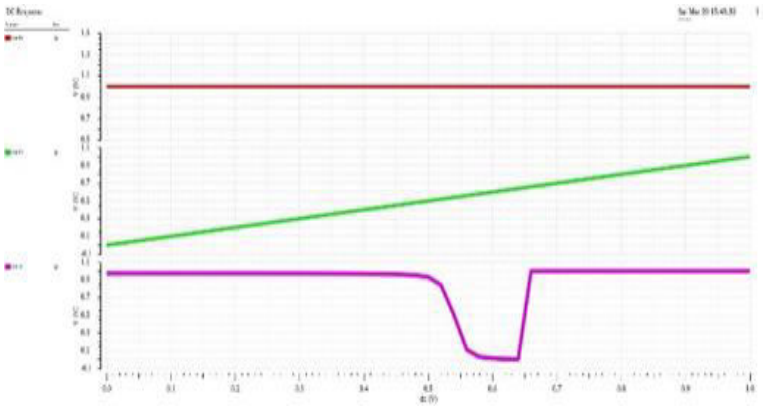

Fig. 14. DC Analysis

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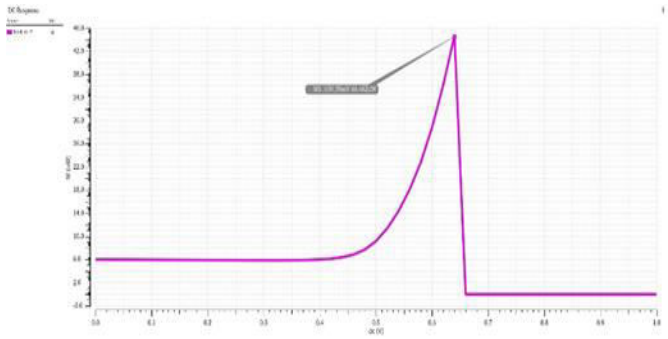

Fig. 15. Total Power

Table I: Performance Parameter of TSPC FF

Performance Parameter	Value
Clock Period	2.5ms
Data Period	10ms
Delay Time	1.168ms
Hold Time	2.5ms
Setup Time	2.5ms
Total Power	44.44Uw

RESULT AND DISCUSSION

Cadence's virtuoso tool was used to simulate the circuits, and the technology used was 180 nm. Cadence Virtuoso's ADEL window was used to calculate the delay and power consumption. The overall power consumption was estimated, which included averaging the dynamic power, which was the most important aspect, as well as the leaky power. The TSPC FF design's setup and hold times are calculated.

CONCLUSION AND FUTURE SCOPE

This article looked at existing flip flop designs. The working of fifteen transistors Flip- flop having low power and high speed has also been demonstrated. Major goal of TSPC FF was to eliminate the LRFF's discharge routes and improvement has been done for the characteristic of dynamic power consumption. The simulations were run at 180 nm, and the designs' functionality was confirmed. The average power usage and delay were estimated and compared amongst the different designs. In addition, the setup and the hold times were calculated and compared to other designs. All of the characteristics showed that the proposed design was superior to all of the other designs.

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