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Application of Multilevel Phase Detector for Clock And Recovery Circuits

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ABSTRACT

For clock and data recovery circuits that are half-rate bang-bang, this article suggests a phase detector (HR-BB-PD) with a number of decision levels. By combining these two methods, the oscillator can run at a data rate that is half that of the input rate while still displaying the size and direction of the PD inputs phase shift. In comparison to a normal two-levels HR BB PD, there is up to 30% reduced output clock jitter. This is because the oscillator's frequency in the phase locked loop of the clock and data recovery circuit may be adjusted more precisely. This enables a bit error rate reduction of up to 5dB in a 5-Gb/s clock and data recovery circuit. A 28-nm FDSOI CMOS device with a supply voltage of 1 V and average power consumption of under 76 W was used to implement the suggested architecture. Despite the highly exciting outcomes of several PLL-based CDRs that have already proposed multilevel (ML) BB PDs, an HR system necessitates a specific PD design. This brief article provides the multi-level (ML-HR-BB-PD).

Keywords: CDR circuits, Multi Level half rate phase detector (ML-HR-PD), PLL, CMOS.

INTRODUCTION

Integrated circuits (ICs) are creating using process very-large-scale integration by packing tens of thousands of transistors onto a single chip (VLSI). VLSI was created in the 1970s, during this period of time communication technologies and advanced semiconductor were being developed. The microprocessor may be categorised as a VLSI device. The bulk of integrated circuits (ICs) could only perform a limited number of jobs before the invention of VLSI technology. A computer circuit may have a RAM, ROM, CPU, and additional glue logic. All of these may be incorporated into a single chip thanks to VLSI. Over the past few decades, the electronics sector has experienced tremendous expansion, mostly as a result of the quick development of applications for large-scale integration (LSI) technologies and system architecture. With the advent of very large scale integration (VLSI) designs, the use of integrated circuits (ICs) in various field like controls, high-performance computing, image and video processing, telecommunications, and consumer electronics has dramatically grown. End customers can access a staggering variety of applications, computational power, and portability thanks to contemporary cutting-edge technologies. Examples include cellular communications and high-resolution, and low-bit-rate video. This trend is predicted to pick up speed and have a significant impact on how VLSI design and system design are done.

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The diagram below depicts the design path for VLSI IC circuits. The many design levels are identified by numbers, and the blocks depict the various steps in the design flow. The requirements, which come first, detail the architecture functionality, and interface of the digital IC circuit that needs to be built.

Using the resultant behavioural description, the design is then evaluated for performance, functionality, adherence to set standards of the devices, and other requirements. Using HDLs, Register Transistor Logic (RTL) description is performed. To evaluate functionality, this RTL description has been emulated. From this point on, EDA tools are required. The RTL description are translated using the tool Logic synthesis into a gate-level netlist in HDL code. A gate-level netlist in HDL is a representation of the circuit's gates and connections, which are constructed in accordance with the timing, power, and area requirements. The process ends with the creation of a physical layout, which is checked before being sent for manufacture.

For combining board layout connectivity and package information with the electrical model of the IC layout parasitic, the Virtuoso System Design Platform delivers time savings and enables IC engineers to easily incorporate layout for system-level parasitic in the IC verification phase. A testbench for the final circuit-level simulation may then be easily constructed using the resulting "system-aware" schematic that is automatically built. The Virtuoso is a System Design Platform has eliminated the labour-intensive for IC designers. A frequency mixer, analogue multiplier, or logic circuit known as a phase detector [1] or phase comparator produces a signal that signifies the phase difference between two signal inputs. Clock and data recovery is a vital feature from optical to electrical communications of many serial communication systems, but especially for high-speed signalling (CDR) [2-3]. The effectiveness of the clock recovery is essential for the communication system's dependability, especially while carrying out synchronous activities like retiming and input data demodulation. Phase noise is produced as a result of the oscillator's oscillator phase variation from ideal. The major goal of this is that we have decided to use this project, titled "Application of Multilevel Phase Detector for Clock and Recovery Circuit [4-7]," to put our creative ideas into practise. The fundamental idea that will come out of our research is handling items that are taller than a specific height.

A proposed half-rate bang-bang phase detector (HRBBPD) with many judgement levels for CDR circuits. Combining these two techniques enables the oscillator to operate at a data rate that is half that of the input while revealing details about the direction and size of the phase shift between inputs of phase detector. This provides more accurate control of the oscillator's frequency in the phase locked loop (PLL) of the clock and data recovery (CDR) circuit.

Schematic design

Three distinct blocks are required to implement the suggested Multilevel-Half Rate-Phase Detector: D-Flip-Flop, XOR gates, and AND gates are examples.

D-Flip Flop

The D flip-flop is a single-bit storage digital device or clocked controlled flip-flop with a single digital input “D". When a D flip-flop is clocked, its output always corresponds to the state of the letter "D" i.e. 0(output) for 0 (input) and 1 (output) for 1 (input). In D Flip Flop, just the two inputs

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D and clock pulse CP are available. When D equals 1, the circuit is in the set state, and the Q output also becomes 1. If D is 0, output Q changes to 0 and the circuit enters a clear state or reset.

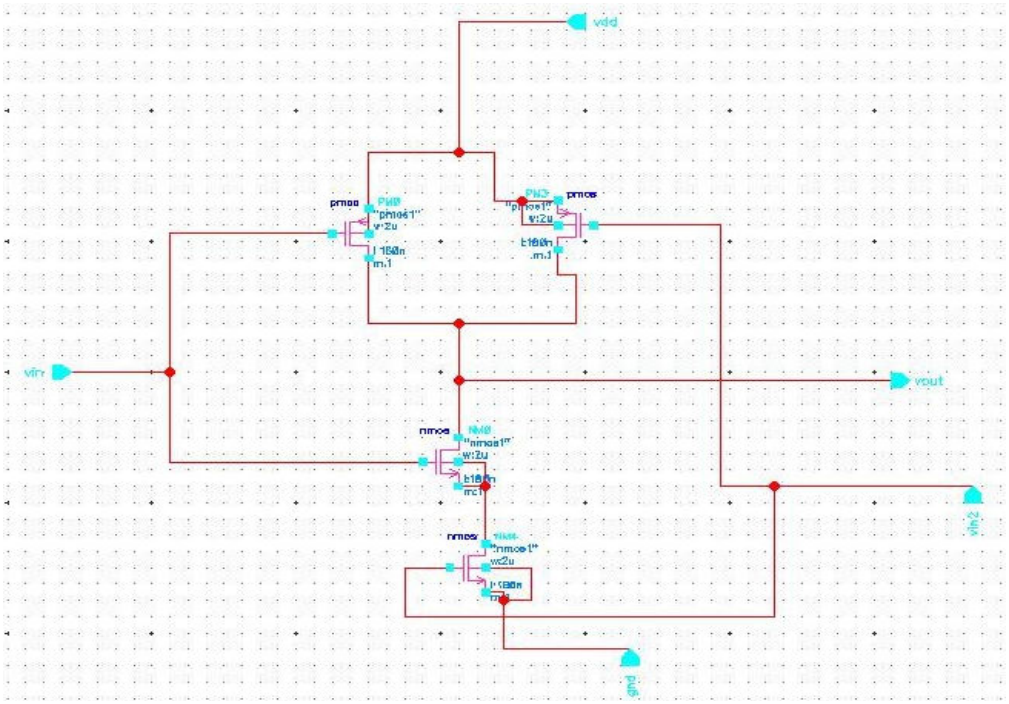

Figure 1 CMOS implementation of NAND Gate

Fig. 1 represents the two inputs NAND gate using complementary metal oxide semiconductors (CMOS) PMOS and NMOS, synthesized by CADENCE virtuoso. This circuit is a basic building block for the implementation of all the digital systems required in this article. As the NAND gate is a universal gate so we can use this gate to synthesize any logic circuits.

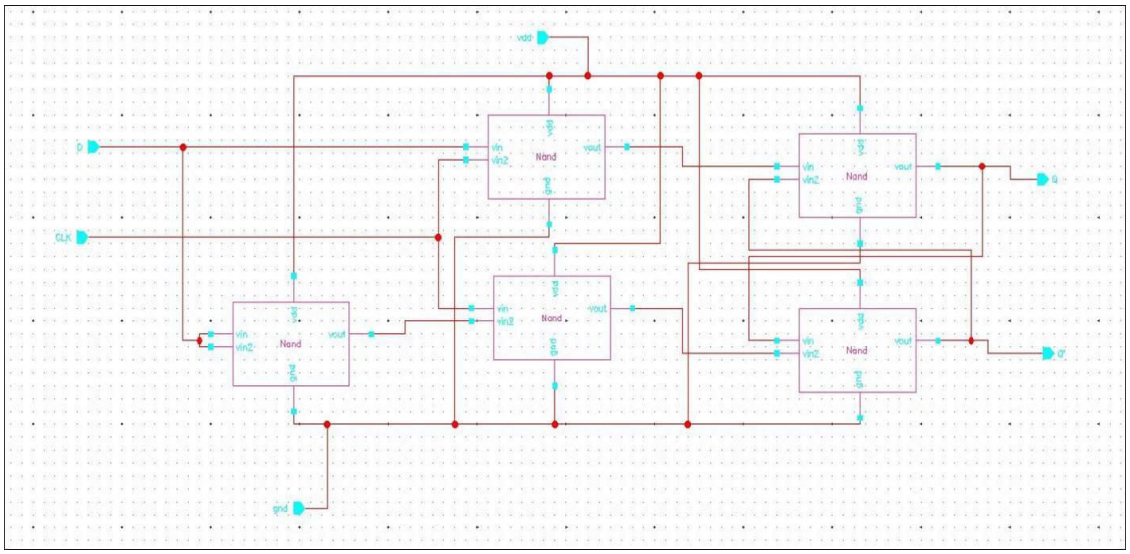

Figure 2 Implementation of D-flip flop using NAND gates

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Figure 2 presents the D flip flop (DFF) conceptual design using NAND gate. It has been put into practise using a straightforward true-single-phase clock edge-triggered CMOS DFF, which enables high-speed flip-flop operation with minimum power consumption (usually 64.7 W @ 10-GHz frequency).

XOR gate:
It performs as a single output, multiple input digital logic gate.
If both of the inputs to the XOR gate are True, the output will be False; otherwise, it will be True.

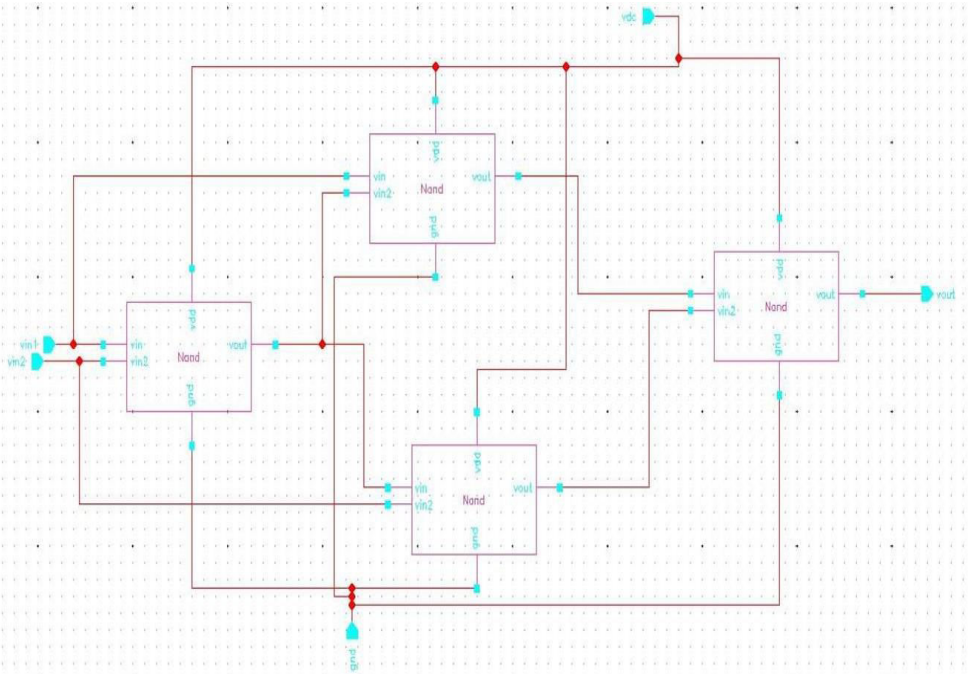

Figure 3 XOR gate implementation using NAND gates

An architecture based on transmission gates has been utilised to build the XOR gates (Fig. 3).
Figure 3 illustrates how the XOR circuit uses CMOS transmission gates (NAND) to accomplish the XOR function.

AND gate:
The term "AND gate" refers to a logic gate that has at least two inputs and one output. In this gate, if one of the inputs is low, the output is also low (zero). The inputs must all be high for the output to be high. The commonly used AND gate have two and three inputs, respectively, even though any number of inputs can be used with it.

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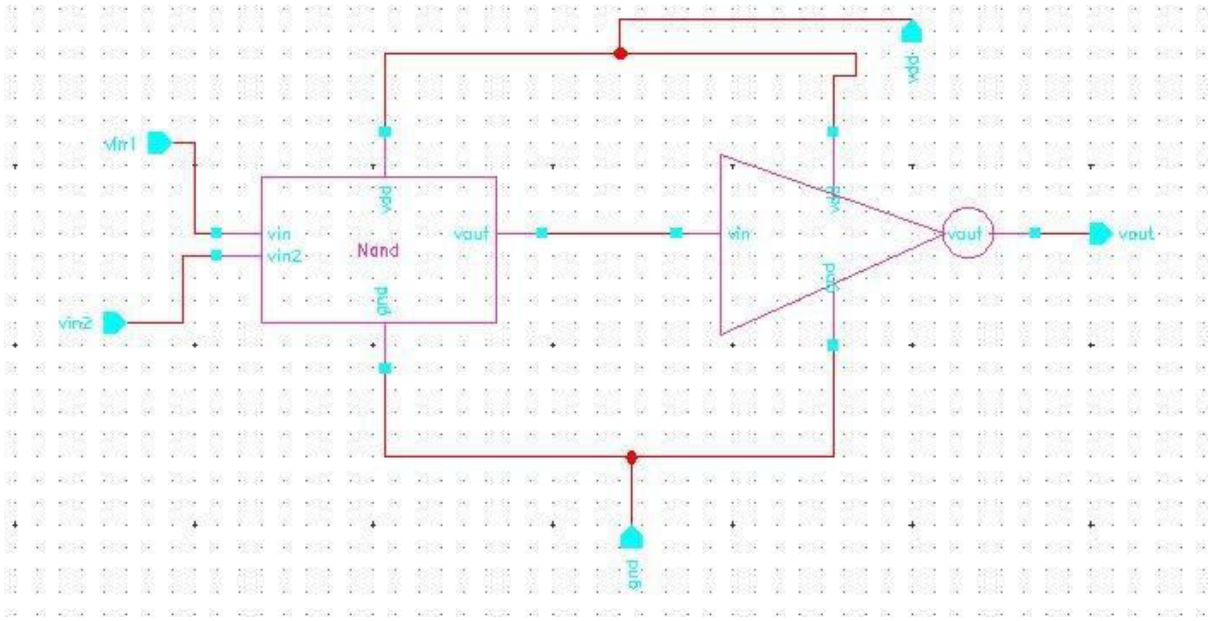

Figure 4 Implementation of AND gate using NAND and NOT

Fig. 4 represents the two inputs AND gate using as synthesized NAND gate and NOT gate, synthesized by CADENCE virtuoso.

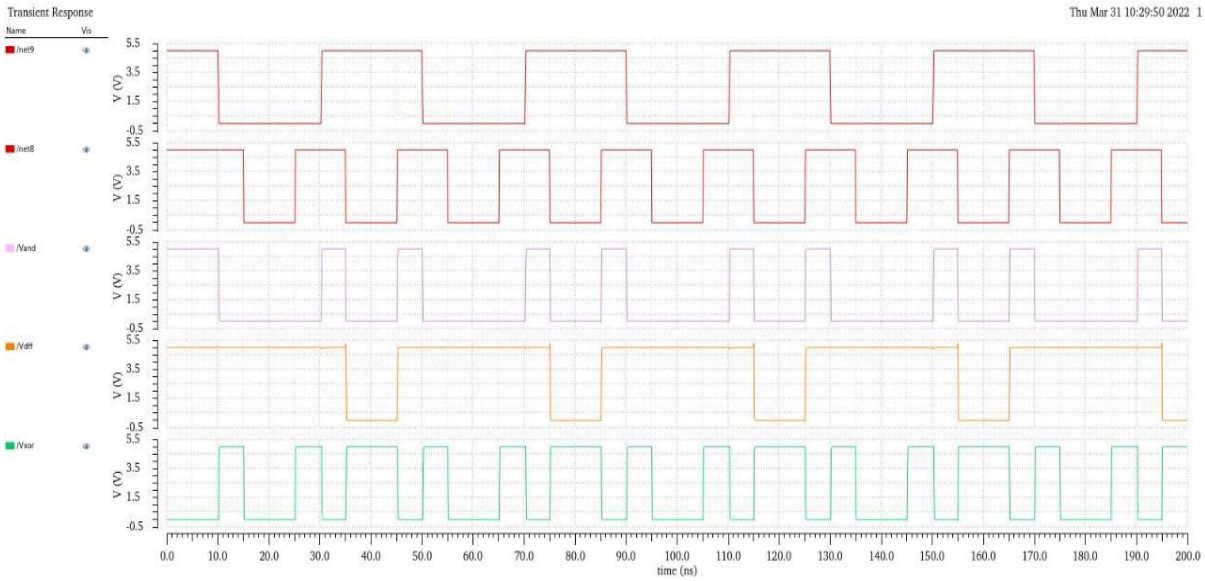

Figure 5 Combined waveforms of D-Flip Flop, XOR, AND gates

Fig. 5 represents the combined transient response of D-Flip Flop, XOR, and AND gates by supplying the corresponding inputs.

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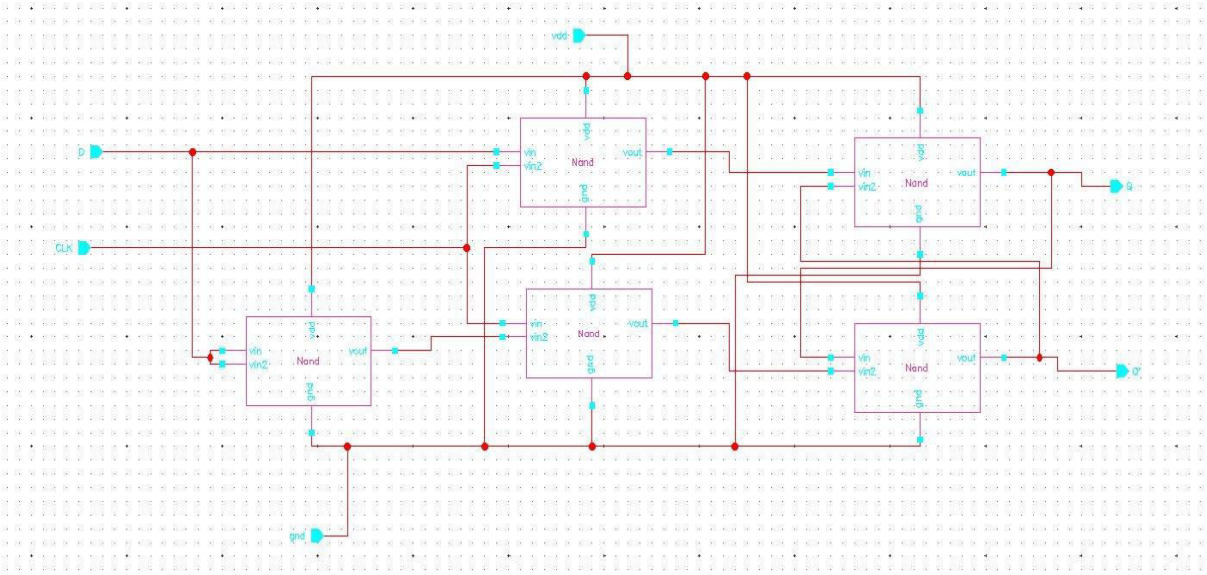

Figure 6 Implementation of the Conventional HR-BBPD using D-FF

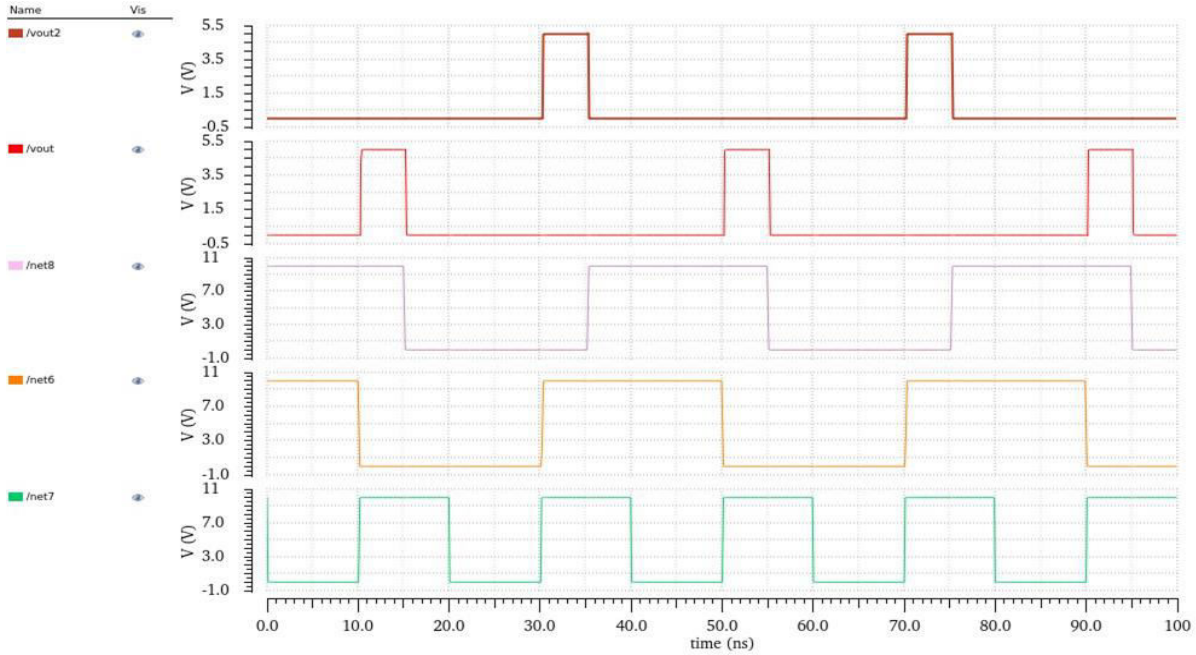

Figure 7 Transient response of as-synthesized Conventional HR-BBPD

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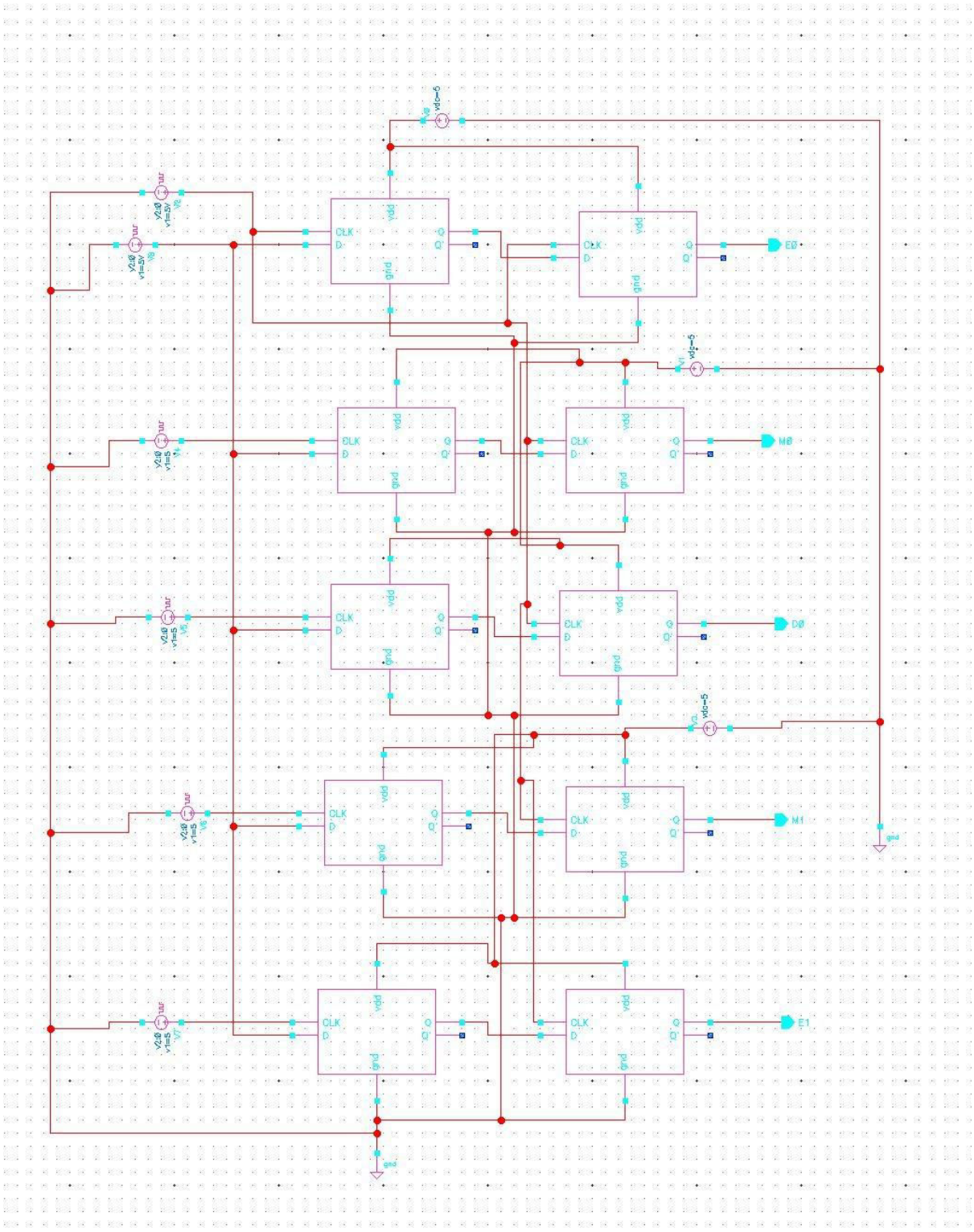

Figure 8 Implementation of the Conventional ML-BBPD using as implemented D Flip-Flops

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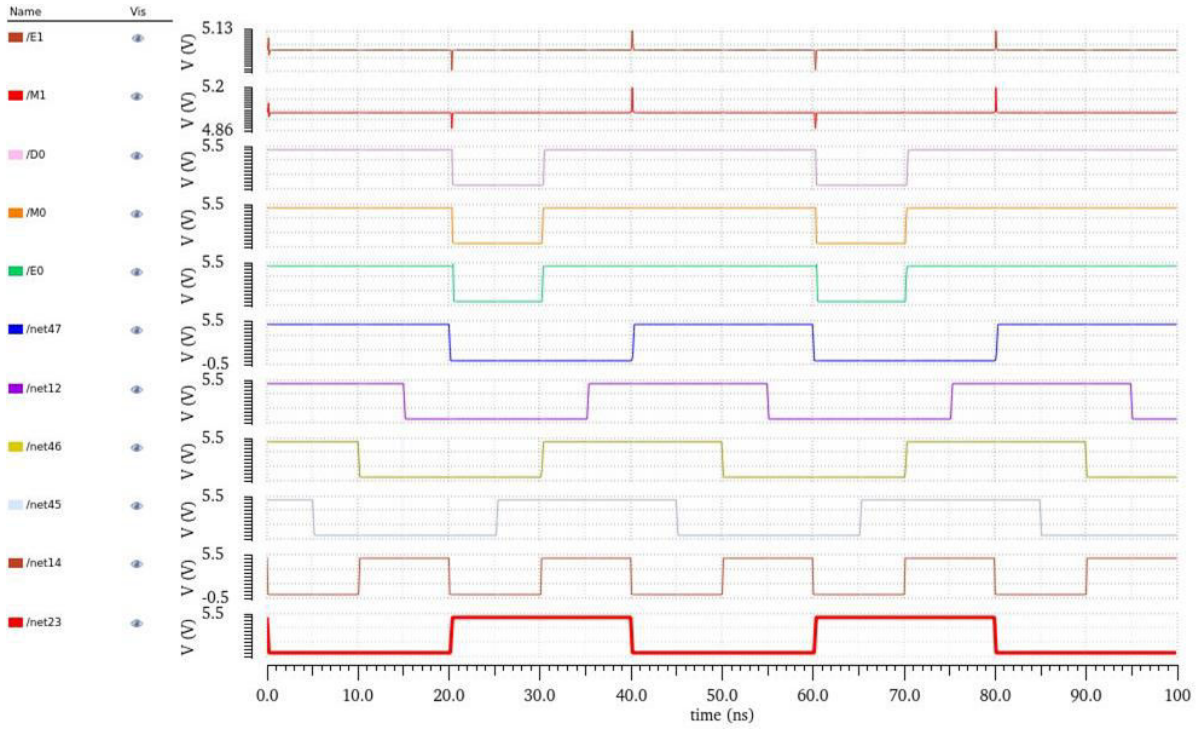

Figure 9 Transient response of the Conventional ML-BBPD

When the clock is behind or ahead of the data, samples are taken. The clock is early and the clock frequency needs to be reduced if the sample obtained by phases 0° and 180° differs while the sample obtained by phases 180° and 90° is the same (transition between phases 0° and 90°)[8-10]. Conversely, if the samples taken by phases 0° and 180° and phases 90° and 180° diverge (the transition between phases 90° and 180°), the clock is running late and the frequency of the clock needs to be increased. Both Early and Late are equal to 0° and no action is taken if there is no transition between phases 0° and 180°, i.e., no data transition [11-12]. This can be summed up as

- Early : E0 Xor E1 =1, E1 Xor D0 = 0 -> clock frequency(decrease) [13]
- Late: E0 Xor E1=1, E1 Xor D0 =1 -> clock frequency(increase) [13]
- Other: E0 Xor E1 =0, clock not adjusted.

Conclusion

An ML-HR-BBPD is recommended in this brief. It offers several levels of quantization to control the VCO and monitor the phase difference in a PLL implementation, providing a good compromise between pure linear and pure BB HR-PD. We determine that the ML-HR-PD retains all the advantages of the HR-BBPD at the expense of a little bit more complexity, while also reducing the jitter of the generated clock because of the finer control of the VCO.

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