Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

Performance Analysis of Gate All Around TFETs for Low Power Circuits

[1]Chetna Bisht, [2]Varun Mishra, [3]Vikas Rathi, [4]Ms Ayushi Jain

[1, 2, 3]Graphic Era (Deemed to be University), Dehradun, Uttarakhand
[4]Assistant Professor, Department of Computer Science and Engineering, Graphic Era Hill University, Dehradun

ABSTRACT

On scaling down MOSFETs below 20 nm or so, it introduces several problems such as drain induced barrier lowering, high OFF-state current due to thinning of gate oxide, and other effects generally known as short channel effects. Keeping these faults into considerations, the market has evolved around several MOSFET like devices including Tunnel-field-effect transistors (TFETs). TFETs has significantly emerged as the substitute to MOSFETs. The TFET belongs to so-called steep-slope devices family because of its ability of scaling down the threshold voltage and VDD beyond the limits of basic CMOS. In this work we investigate the constant current mirror circuit level performance of gate-all-around TFETs and comparison has been drawn with the conventional MOSFET circuit. It is observed that TFET based current mirror circuit outperforms MOSFET based circuit. Therefore, TFETs can be utilized as a better candidate instead of MOSFET for low power circuit designing.

Keywords: Tunnel-field-effect transistors, gate-all-around, current mirror

INTRODUCTION

An ideal MOSFET's basic functionality depends on the electrical variations in the channel width along with the flow of carriers that can either be electrons or holes. The width of the channel is controlled by the voltage on the gate. MOSFET is the most basic and core component in the integrated circuit technology. The introduction of the MOSFET device has taken a change in the realm of **switching in electronics.** But, when we are trying to scale down our MOSFETs somewhat below 20 nm, we come across several problems related to synthesis, fabrication, leakage current, SS - subthreshold swing, DIBL - drain-induced barrier lowering, and other various short channel effects (SCE) [1, 2]. These challenges of MOSFETs in nanoscale regime validates our motive to use tunnel-field-effect transistor keeping its established property into consideration [3, 4]. TFET is also constructed in the same manner as MOSFET but here in TFET doping of source and drain terminals is of reversed type. TFETs provides low leakage current by making use of interband tunnelling at source-channel junction. When under OFF state condition, TFETs has relatively higher barrier for the minority carriers which leads to negligible leakage current due to the injecting of minority carriers. Apart from these pros, TFETs derives low drive current, high ambipolar current and threshold voltage [5]. In order to overcome these, GAA – gate all around structures are used which in turn enhances the control over the channel. GAA are modified

Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

transistor structure where the channel is contacted with gate from all sides, enabling continued scaling [6]. These transistors employ stacking of two layers one above the other. This work has been widely divided into sections including the introduction to TFETs followed by the device description in the second section in which the device parameters are overviewed and examined. The tool used for this purpose is Silvaco Atlas [7, 8]. The third section comprises of the circuit implementation which has been carried out using Verilog A in Cadence environment [9]. The last section gives the conclusion of our work with all the discussions.

DEVICE DESCRIPTION

Fig.1 shows the 2-D lateral structure of the device, which clearly displays that the general construction has a double gate, which provides a better controllability over the channel and helps in improving the stability, power and ON-OFF current of the device. A closer look at the device reveals that the tunnelling occurs at the source – channel interface between 15 to 30nm along the channel. The channel length is kept 50nm which is sufficient enough to provide higher I_{on} current.

The TCAD tool Silvaco Atlas has been used to carry out of the numerical evaluations for the given device. The model used for simulation are Concentration-dependent mobility model, Shockley-Read-Hall recombination model, Band gap narrowing model, Field dependent mobility model, Auger recombination model, and Kane's band to band tunneling model [10].

The channel length is kept as 50nm. The source length and drain length are 20nm each. The source doping is 10^{20} cm^{-3} of p-type and the drain doping is 5 x 10^{8} cm^{-3} of n-type. The channel doping is 10^{16} cm^{-3} of n-type as well.

After the analysis we observed that V_T is 0.266325 V and the subthreshold swing is 31.8091 mV/dec. Further calculating, the transconductance (g_m) is 4.36076 x 10^{-5}. The I_{ON} is observed to be 1.01813e^{-5} and I_{OFF} is 3.38489e^{-15}. The I_{ON} / I_{OFF} ratio is 3.00786 x 10^{9}.

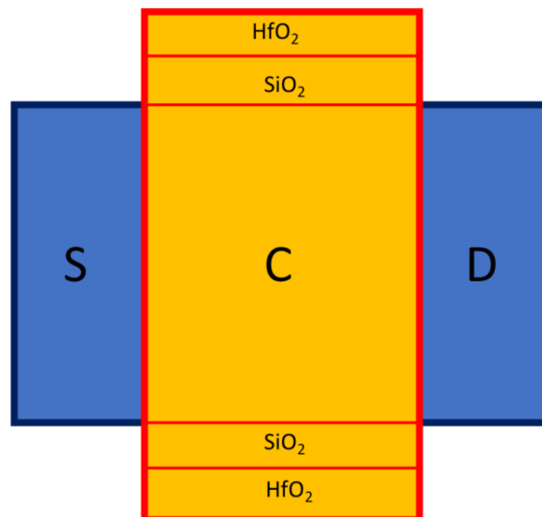

Fig.1 2-D schematic representation of GAA-TFET.

Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

CIRCUIT IMPLEMENTATION

The device has very fairly outstood our expected results and it is seen that the problems we've discussed in the case for MOSFET are sufficiently solved. Moving to the second part of our objective, a lookup table consisting of all the parameters of our device was being designed. Further using this lookup table, the device was implemented at circuit level using Verilog A in Cadence environment. A test circuit was studied with the same efficient parameters as that of our device level study. Fig. 2(a) and (b) shows the test circuit of the device and graphs shows comparison of the analysis at both device and circuit level. As a result, we found that our model effectively shows responses at circuit level as well. We operated our test circuit at a supply voltage of 1V and the DC analysis were performed which were then matched with the graph that was extracted from the device study in Silvaco Atlas. Both the results matched significantly hence validating the persistence of our device.

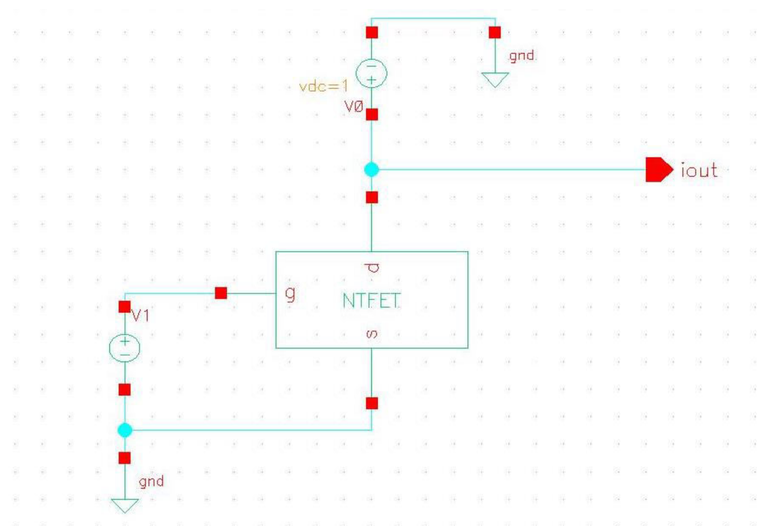

Fig. 2(a) DC analysis of proposed GAA-TFET.

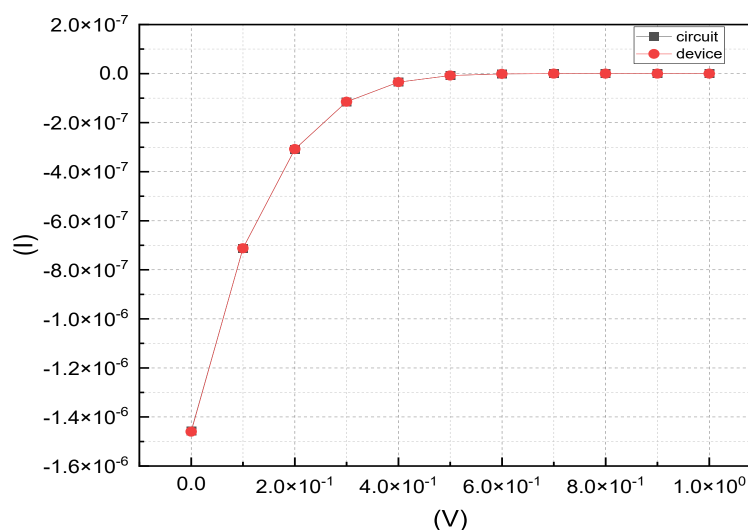

Fig.2(b) Comparison analysis at both device and circuit level

Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

We tried to implement our device for basic electronic circuit. We have studied the basic characteristics of a current mirror. A current mirror is circuit in which we aim to replicate the input current of one active device to the respective output of the other active devices [11]. We can also term this as an ideal current amplifier including the inverting design that can upturn the current flow direction. The Fig. 3 shows a basic representation of a current mirror through which we can simply state that : $\mathbf{I_{ref} = I_{copy}}$.

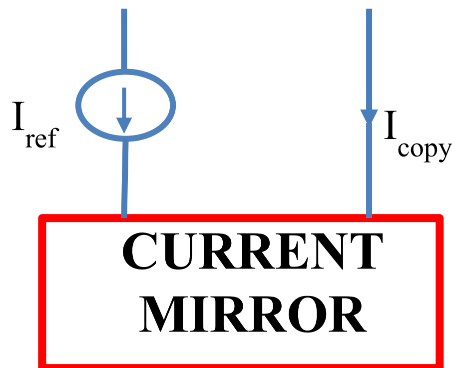

Fig. 3 Basic current mirror.

We have designed a current mirror using MOS technology. The parameters incorporated are :

NODE	COMPONENT	UNITS
In terms of input	Vdc	800mV
In terms of input	Idc	1uA
In terms of output	Vdc	1V

Fig. 4 (a) and (b) shows a schematic of basic current mirror and DC response of the same.

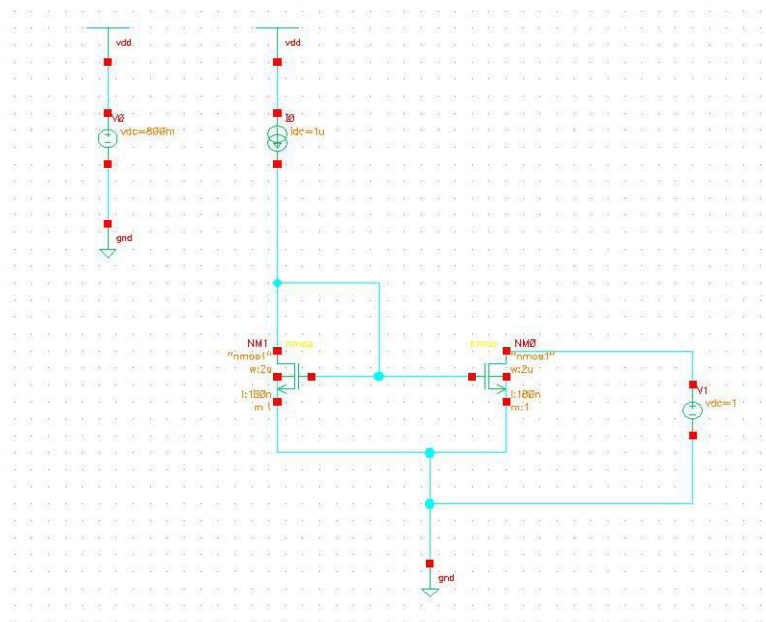

Fig. 4(a) Schematic of current mirror using basic MOS technology

Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

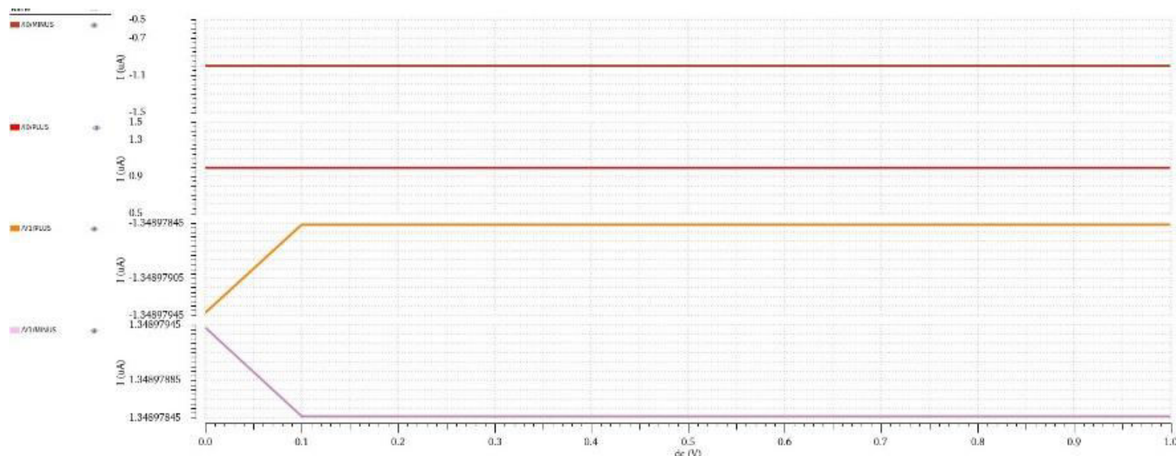

Fig. 4(b) DC response of basic current mirror

This MOS based circuit was able to withstand the basic operating principle of a current mirror. The current derived at the output node was same as that at the input node. Further designing the same current mirror using our model in place of basic MOS. The parameters were same as previously mentioned for basic MOS current mirror. Fig. 5 (a) and (b) shows the schematic of the current mirror using TFET and the DC response of the same. This circuit also stood by the current mirror's objective of replicating the current.

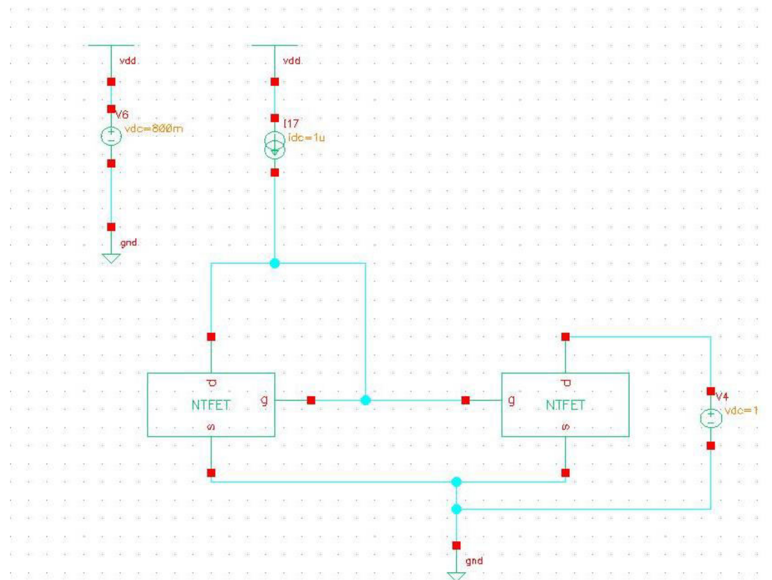

Fig. 5(a) Schematic of the current mirror using TFET

Webology, Volume 18, Number 2, 2021
ISSN: 1735-188X
DOI: 10.29121/WEB/V18I2/43

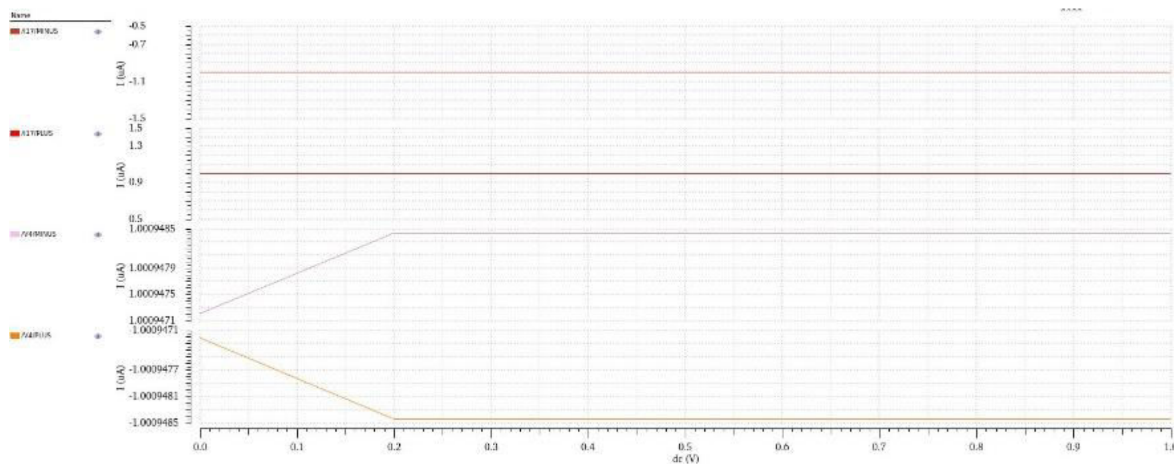

Fig. 5(b) DC response of the current mirror using TFET

CONCLUSIONS

Through this work we have proposed a GAA TFET structure which can be used as the substitute of a MOSFET. We have tried to frame our device both in device level and circuit level. We have observed that our device has shown expected results in terms of power consumption and the output derivation in the referred circuit. As a result, we can term V_T as 0.266325 V and the subthreshold swing is 31.8091 mV/dec. The transconductance (g_m) is 4.3607 x 10^{-5}. The I_{ON} is observed to be 1.01813e^{-5} and I_{OFF} is 3.38489e^{-15}. The I_{ON} / I_{OFF} ratio is 3.00786 x 10^9. The current mirror upholds it's basic objective both using MOS and TFET. This validates our objective of proposing TFET in place of MOSFET. Further we aim to improve it to a better level in terms of issues like leakage current, SS, DIBL, short channel effects as well as fabrication and synthesis.

REFERENCES

1. Frank, D. J., Dennard, R. H., Nowak, E., Solomon, P. M., & Wong, H.-S. P. (2001). Device Scaling Limits of Si MOSFETs and Their Application Dependencies.
2. Roy, K., Mukhopadhyay, S., & Mahmoodi-Meimand, H. (2003). Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. Proceedings of the IEEE, 91(2), 305–327. https://doi.org/10.1109/JPROC.2002.808156
3. Seabaugh, A. C., & Zhang, Q. (2010). Low-voltage tunnel transistors for beyond CMOS logic. Proceedings of the IEEE, 98(12), 2095–2110. https://doi.org/10.1109/JPROC.2010.2070470
4. Koswatta, S. O., Lundstrom, M. S., & Nikonov, D. E. (2009). Performance comparison between p-i-n tunneling transistors and conventional MOSFETs. IEEE Transactions on Electron Devices, 56(3), 456–465. https://doi.org/10.1109/TED.2008.2011934
5. Sant, S., Moselund, K., Cutaia, D., Schmid, H., Borg, M., Riel, H., & Schenk, A. (2016). Lateral InAs/Si p-Type Tunnel FETs Integrated on Si - Part 2: Simulation Study of the Impact of Interface Traps. IEEE Transactions on Electron Devices, 63(11), 4240–4247. https://doi.org/10.1109/TED.2016.2612484
6. Verhulst, A. S., Sorée, B., Leonelli, D., Vandenberghe, W. G., & Groeseneken, G. (2010). Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor. Journal of Applied Physics, 107(2). https://doi.org/10.1063/1.3277044 Silvaco TCAD User's Manual (2019)

7. Tripathy, M. R., Singh, A. K., Samad, A., Chander, S., Baral, K., Singh, P. K., & Jit, S. (2020). Device and Circuit-Level Assessment of GaSb/Si Heterojunction Vertical Tunnel-FET for Low-Power Applications. IEEE Transactions on Electron Devices, 67(3), 1285–1292. https://doi.org/10.1109/TED.2020.2964428
8. Kumar, D., Rahi, S. B., & Kuchhal, P. (2021). Investigation of Analog Parameters and Miller Capacitance Affecting the Circuit Performance of Double Gate Tunnel Field Effect Transistors (pp. 335–349). https://doi.org/10.1007/978-981-16-1510-8_33
9. Mishra, V., Verma, Y. K., & Gupta, S. K. (2019). Investigation of localized charges on linearity and distortion performance of ferroelectric dual material gate all around TFETs. Journal of Nano- and Electronic Physics, 11(4). https://doi.org/10.21272/jnep.11(4).04014
10. Vidhate, A. D., & Suman, S. (2021). Low Power High Performance Current Mirror - A Review. Journal of Physics: Conference Series, 1804(1). https://doi.org/10.1088/1742-6596/1804/1/012161